Silicon-On-Glass MEMS

Design

Handbook

***A** Process Module for a Multi-User Service Program*

A Michigan Nanofabrication Facility process at the University of Michigan

March 2007

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CHAPTER 1

SILICON ON GLASS (SOG) MICROELECTROMECHANICAL SYSTEMS (MEMS) PROCESS

1.1 Introduction

The silicon on glass (SOG) module has been developed to integrate CMOS and high-aspect ratio MEMS sensors and actuators. This is accomplished by forming recesses on a glass wafer, anodically bonding a silicon wafer to that glass wafer, and using deep reactive ion etching to etch MEMS devices through the backside of the silicon wafer over the glass recess. In this initial SOG beta run, CMOS integration will not be offered, only the high-aspect ratio fabrication of the MEMS devices will be offered. Figure 1.1.1 and Figure 1.1.2 show a MEMS device fabricated using the SOG process.

This process and initial beta run is offered through MEMS Exchange. To participate in this run, please register with MEMS Exchange, submit a design and submit the run as a work order through the MEMS Exchange system.

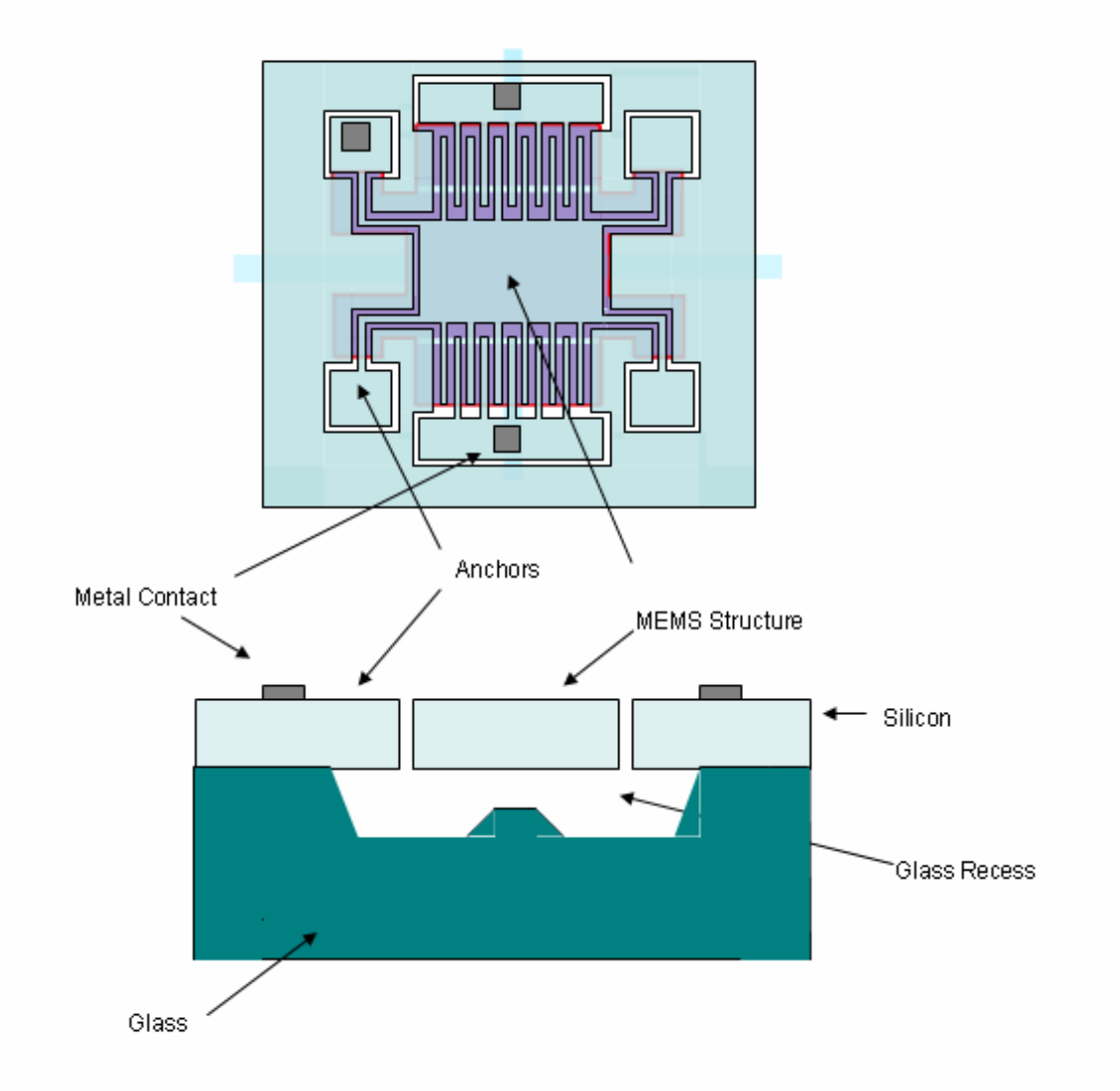


Figure 1.1.1 - Final device shown, top view & cross section

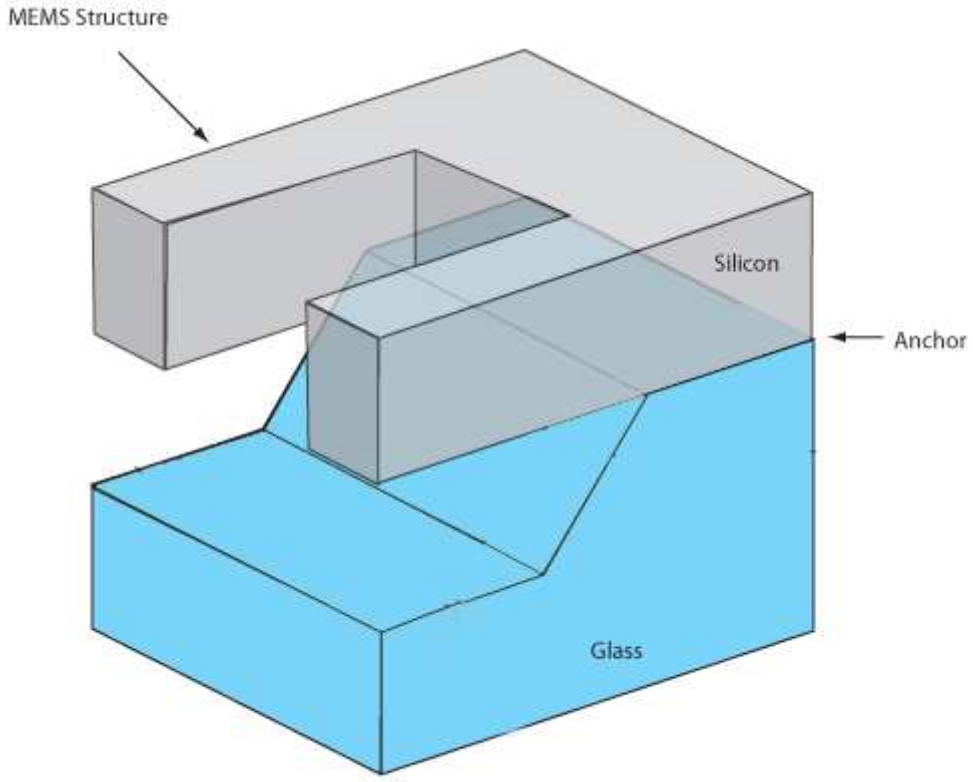
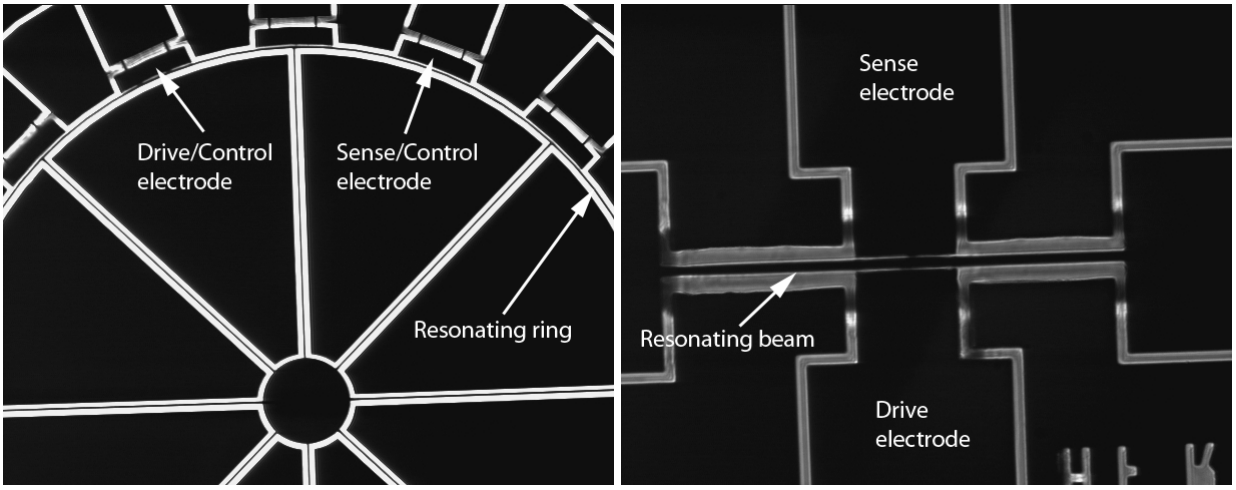


Figure 1.1.2 - Final Device Shown, 3D cross section view



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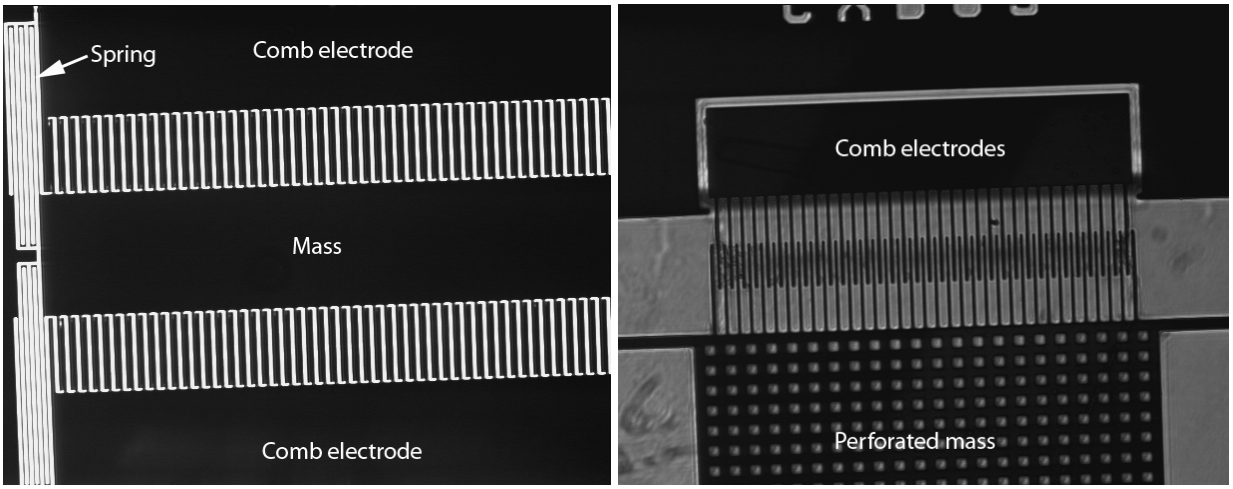


Figure 1.1.3 - (clockwise from top left) Vibrating Ring Gyroscope, Beam Resonator, Perforated Mass with Comb Electrodes, Accelerometer

This process is primarily for capacitive sensors and actuators because the MEMS structures are fabricated by deep reactive ion etching (DRIE) of the bulk silicon. The movement of the structures is in the plane of the wafer. Therefore, electrode pads that connect CMOS and the MEMS externally are fabricated using bulk (low doping) silicon which has high resistance. This must be considered before choosing this process for your CMOS applications

Typical MEMS devices can be accelerometers, gyroscopes and resonators as shown in Figure 1.1.3 but are not limited to these examples. In general, devices that can be fabricated with thick silicon-on-insulator (SOI) technology or devices that can be fabricated using glass-silicon bonding and DRIE steps can be fabricated with this process.

In this chapter, an overview of the process flow is given with cross-sectional views of the substrates. In the next chapter, layout design rules are explained with top view examples relating the process to the mask design drawn using any commercial layout editor, such as MentorGraphics' IC Station and Tanner's Ledit.

1.2 Process Flow

The SOG process is derived from the work of Prof. Khalil Najafi and Dr. Jun Chae at the University of Michigan, which has been geared towards integration of CMOS with capacitive accelerometers. This process flow is capable of integrating CMOS with high-aspect ratio silicon MEMS structures.

In basic terms, this process takes a silicon wafer and a glass wafer that has been processed to form recesses wherever there will be moving silicon structures and bonds them together. Then, by using deep reactive ion etching (DRIE), silicon is selectively etched from the backside of the silicon to form high aspect ratio silicon structures. Because the moving silicon structures are over glass recesses and their anchor points are not, these high aspect ratio silicon structures can be designed to form MEMS devices like accelerometers, gyroscopes, resonators and combdrives.

The MEMS fabrication process of SOG begins with the glass wafer. 10 µm recesses are etched into a 500 µm thick glass wafer using wet chemical etching as shown in Figure 1.2.1. As will be

discussed in the next chapter, undercut of the glass must be considered in the layout. The mask used for this purpose is named GLASS_RECESS. The glass recess should also include temporary anchors for the silicon mass, which will be etched away and released later. These temporary anchors provide extra support structure for the silicon MEMS structures during DRIE, as well as reducing thermal effects during DRIE.

Metal (or conductive) shielding on the glass as shown in Figure 1.2.2 is required to stop the charge build-up on the glass during DRIE. In the final step, silicon will be etched using DRIE. In this step there will be features with different widths on the mask. Unfortunately, they will have different silicon etch rates, narrower patterns having slower etch rates, due to a DRIE effect called microloading. To etch the fine features, the silicon must be over etched so that even the narrowest feature is etched through the whole thickness. While the small features continue to etch, the reactive ions traveling through the already etched large features will accumulate on the insulator below (static charge) and start to repel other ions towards sides of the silicon creating an undercut of the mask and thereby deteriorating the silicon etch profile. By depositing a conductive film in the glass recess, these charges from etch ions can be dissipated to the bulk silicon. The conductive film on glass recess is a 2000Å layer of ITO (Indium Tin Oxide, a transparent conducting oxide) patterned using the same masking layer as GLASS_RECSS. The transparency of the ITO layer makes the inspection of the devices easier. After depositing the ITO, the wafers are anodically bonded together by applying 1000 Volts at around 350 °C as shown in Figure 1.2.3.

The performance of capacitive sensors like accelerometers and gyros is dependant on the gap between the sensing electrodes, the area of the gap, and the mass of the structure. A larger mass is desired most of the time to increase the sensitivity and the resolution of these kinds of devices. However, MEMS wafers have a constant cost per wafer, and to reduce the cost, the size of each device must be reduced. Because the area of the device is very valuable, this large mass can only be produced with a thicker silicon wafer. Though it is desirable to use a thick silicon wafer and the smallest achievable gap possible, there are limitations due to the DRIE. The aspect ratio of DRIE is limited to approximately 50:1, and the smallest achievable gap is approximately 2µm, thus the silicon thickness must be 100µm. However, in this initial beta run, the minimum feature size will be limited to 5 µm and the maximum feature size is 10 µm. In the future, a larger range of feature sizes will be offered as well as processing of full thickness silicon wafers with CMOS.

External electrode pads must be made to make an ohmic contact to these MEMS devices. This is achieved by depositing 0.5 µm aluminum at the backside of the silicon wafer and patterning using a mask named CONTACT as shown in Figure 1.2.4. After this step, the backside of the wafer is patterned in preparation for the DRIE using a mask named SI_MEMS. DRIE etches silicon all the way down to the glass wafer and creates moving high-aspect ratio silicon MEMS structures over the glass recessed areas as shown in Figure 1.2.5. After this step, the dies can be separated dicing them apart in a saw. The temporary glass anchors will secure the silicon MEMS structures during dicing.

After the DRIE is completed, the shielding metal layer is etched away and the entire wafer is diced apart on a saw. The MEMS structures on the individual dies are then released by etching

away the temporary anchors in HF. The resulting structures are critically dried and then are complete.

The following gives a summary of layers related to the SOG process that has been briefly discussed so far. In the next chapter, layout design rules have been explained with demonstrations including the critical issues like silicon islands, glass recesses and shielding metal.

Layers on the Glass

1. Glass recess and shielding metal on glass recess to prevent microloading effect during DRIE.

Layers on the Backside of the Silicon

1. Metal contacts (Aluminum on silicon for external electrical contacts to silicon parts)
2. MEMS device patterned with deep reactive ion etch (DRIE).

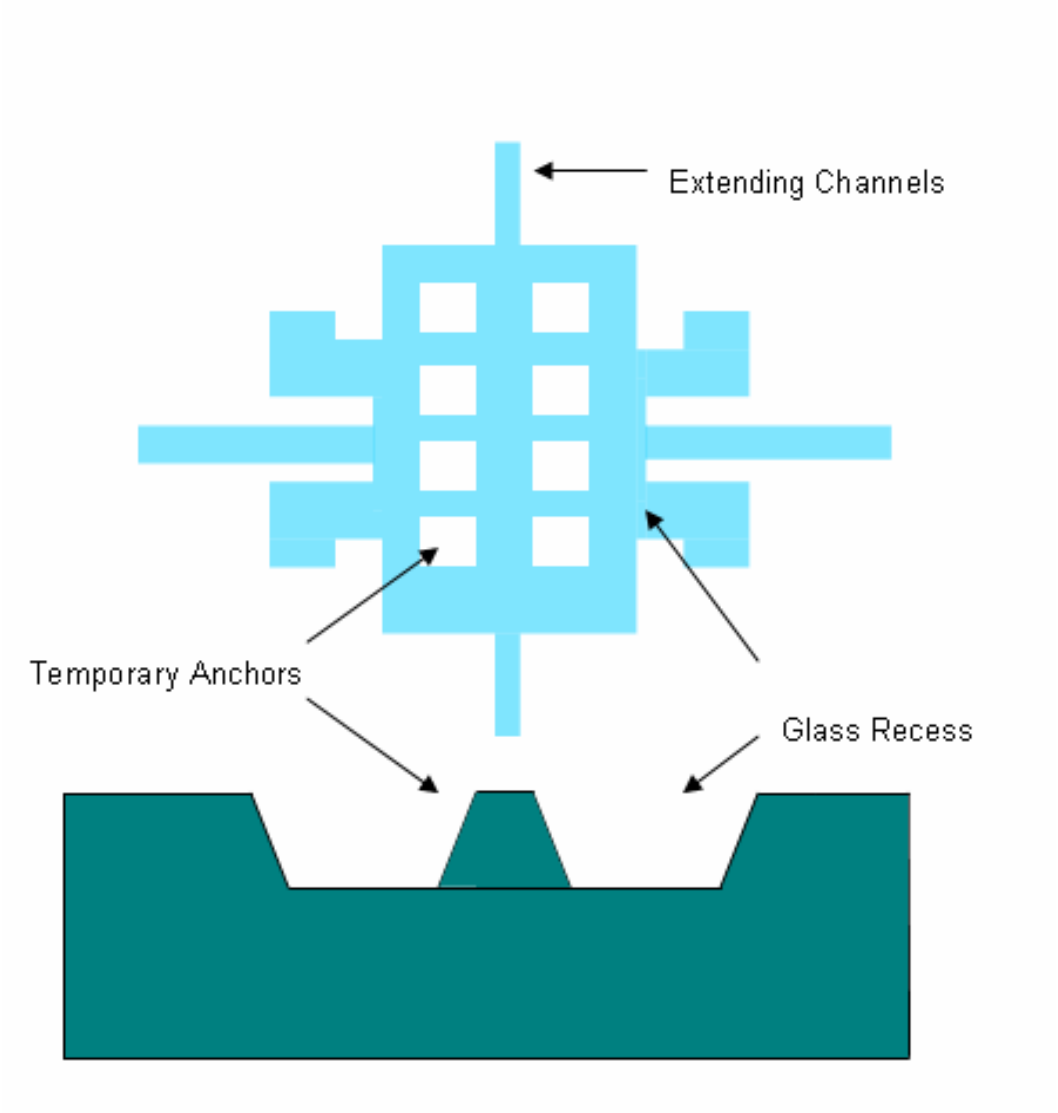


Figure 1.2.1 - On glass, make recesses (10 µm) for moving MEMS parts, while retaining temporary 30 µm anchors. Uses mask GLASS_RECESS.

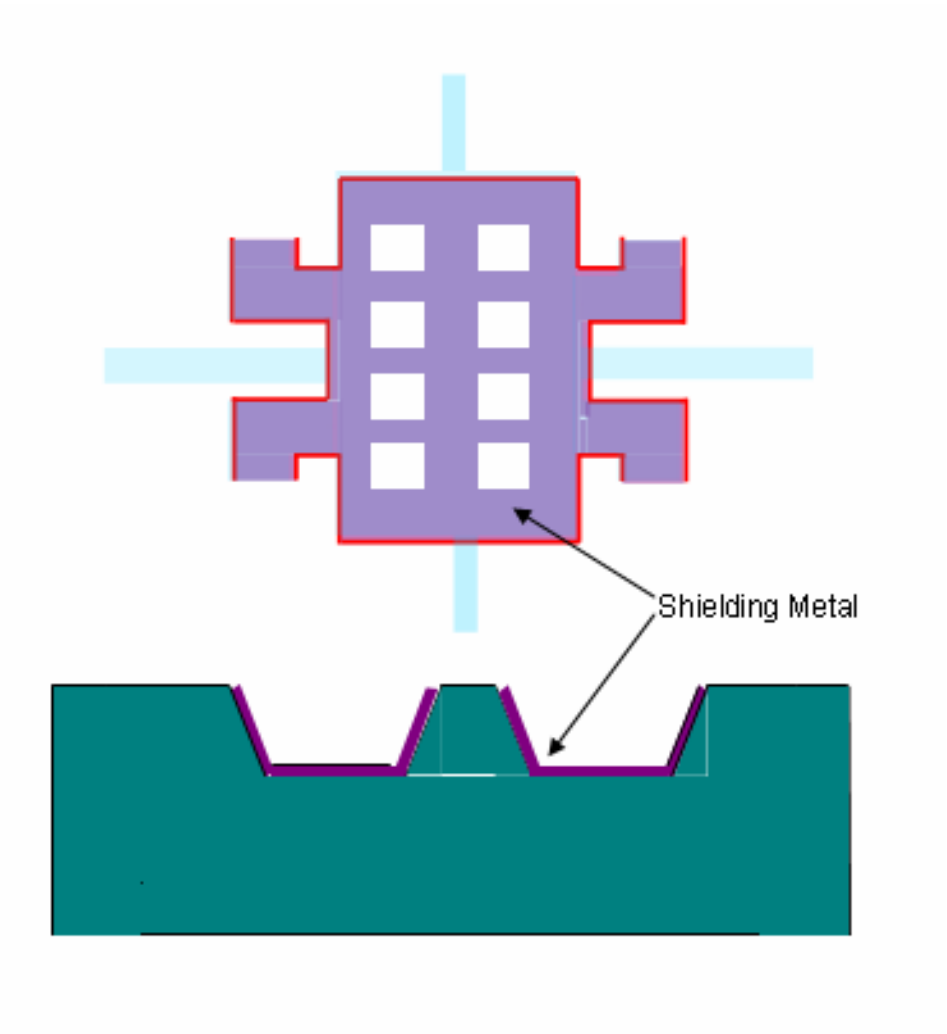


Figure 1.2.2 - Deposit a shielding metal on glass recess to prevent microloading effects during DRIE. Uses previous masking layer GLASS_RECESS.

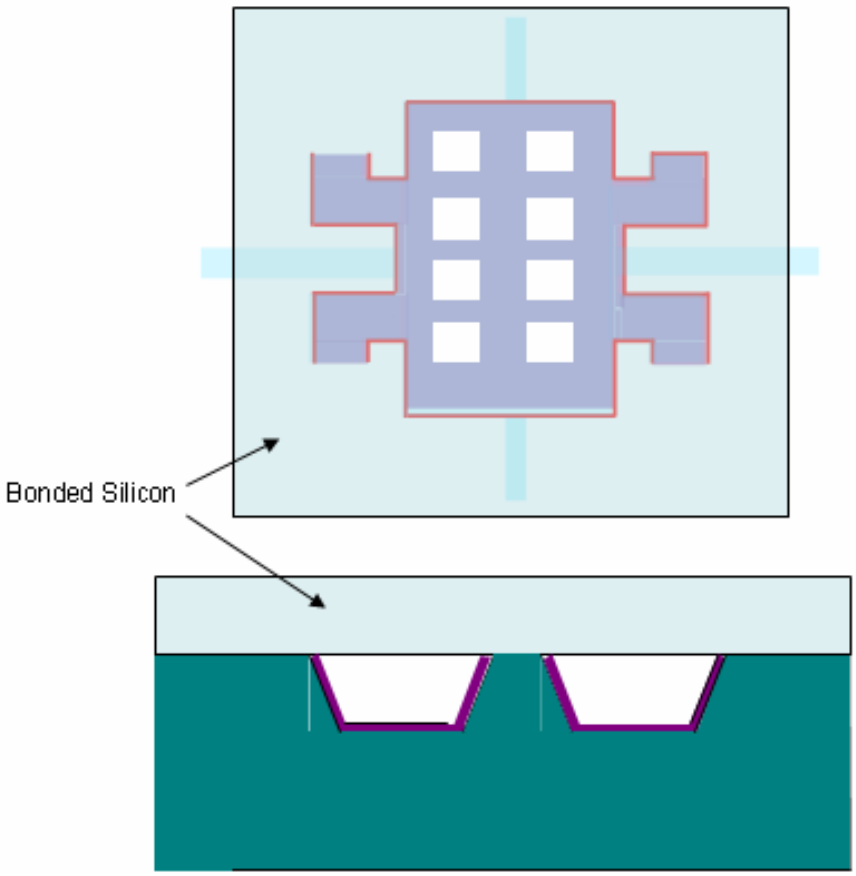


Figure 1.2.3 - Anodically bond a silicon wafer to the front side of the prepared glass wafer. The temporary glass anchors secure the silicon mass and aid in heat transfer during DRIE.

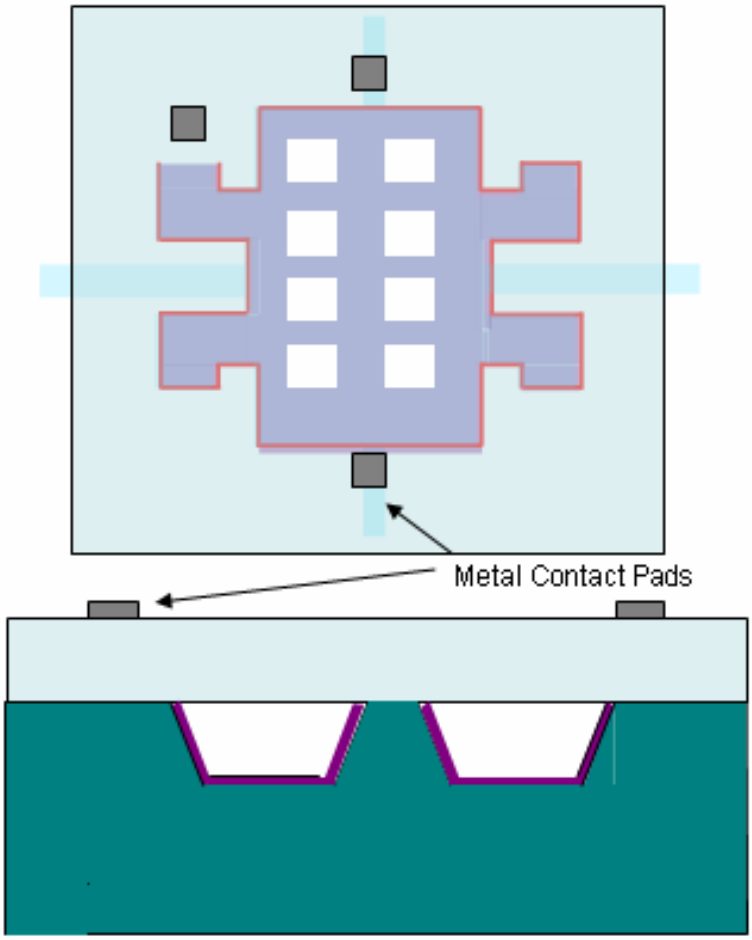


Figure 1.2.4 - Pattern metal contacts (aluminum) on backside of silicon for external conncetions. Uses mask CONTACT.

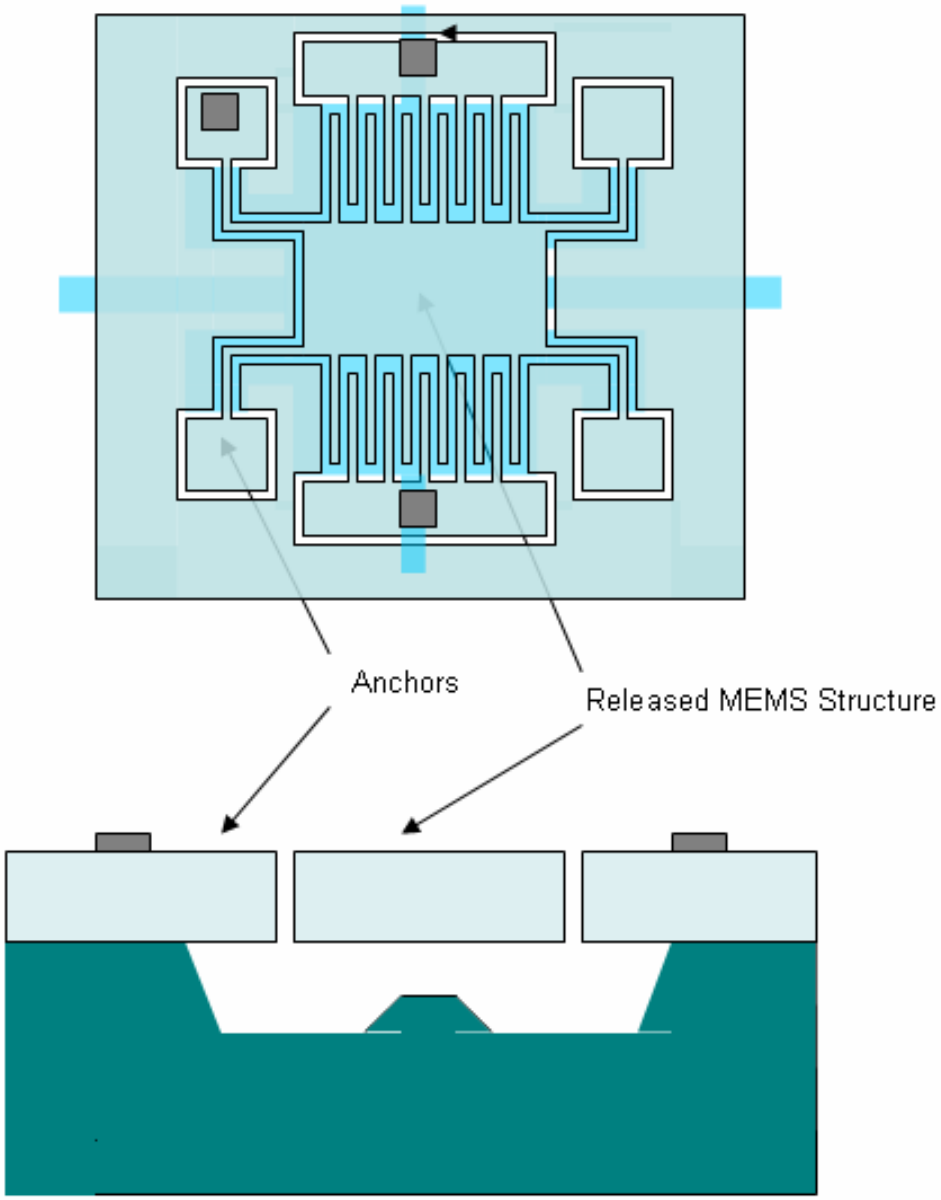


Figure 1.2.5 - DRIE the silicon to form MEMS structures over the glass recess. Uses mask SI_MEMS. After DRIE, the wafer is diced and the silicon is released in HF by etching the temporary glass anchors.

CHAPTER 2

AN OVERVIEW OF THE LAYOUT DESIGN RULES

2.1 Introduction

In this chapter layout design rules are explained in detail with the help of examples. These design rules have been developed from the past fabrication experience and show process limitations and design considerations. Concepts like glass recesses, shielding metal and silicon islands have been explained and pictured in detail. With the help of top view examples, the process flow and cross-sectional drawings shown in the first chapter, these concepts and the understanding of the process should be clear.

Minimum feature sizes reported here are mostly limited by the resolution and alignment capability of the lithography steps and the uniformity and the resolution of the etching tools.

Table 2.1.1 - Table 2.1.4, below, refer to all the relevant information in each layer. Maximum and minimum feature sizes, alignment tolerances and layer registration are defined. Specific design details regarding each layer are specified in the comments.

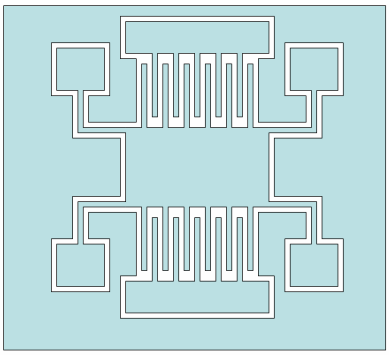
Lithography Level: SI_MEMS	
	Die Size: 0.5 x 0.5 cm
	Minimum Feature Size: 5 µm
	Maximum Feature Size: 10 µm
	Minimum Gap Size: 5 µm
	Minimum Anchor Point Size: 200x200 µm
	Maximum Length: see 2.2.3
	Material: Silicon
	Thickness: 100 µm
	Alignment Tolerance: 5 µm
	GDS Layer Number: 1
	Layer Registration: The SI_MEMS layer aligns to the GLASS_RECESS recess layer. Due to the alignment tolerance of 10um and the undercut of the glass etching, the minimum anchor point size must be at least 200x200 µm. This anchor point must also be at least 100 µm away from the edge of the designed glass recess. The released silicon structure must be at least 10 µm away from the edge of the designed glass recess.
	Comments: The fixed die size for this beta run is set at 0.5 x 0.5cm Try to fill in all extra spaces, leaving a maximum gap of 10 µm. This is to improve the DRIE etch uniformity.

Table 2.1.1 - SI_MEMS Layer

Lithography Level: GLASS_RECESS	
	Minimum Feature Size: 50 µm
	Minimum Gap Size: 50 µm
	Temporary Anchor Size: 30 µm
	Material: Glass
	Etch depth: 10 µm
	Alignment Tolerance: 10 µm
	GDS Layer Number: 2
	Layer Registration: None, first level
	Comments: This layer is for creating the glass recess. The total undercut from the etching process is ~30 µm which dictates the minimum feature size and gaps defined. These recesses must be connected within a die and have extending channels outside of the die (0.5x0.5 cm) at least 200 µm and terminate in the dicing lines (edge of die) for pressure equalization. Temporary anchors must be placed under released silicon masses to aid in DRIE and must be 30 µm, these will later be released in a final HF release.

Table 2.1.2 - GLASS_RECESS Layer

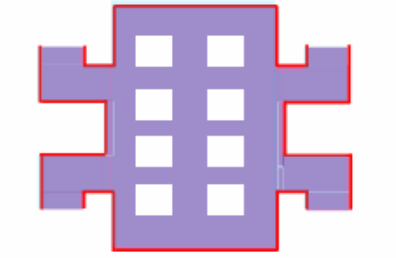
Lithography Level:	
	Comments:
	This layer is for creating the shielding metal in the glass recess which is used to reduce microloading effects during DRIE. The metal is deposited inside the glass recess using the same masking layer as GLASS_RECESS

Table 2.1.3 - Glass Metal Layer

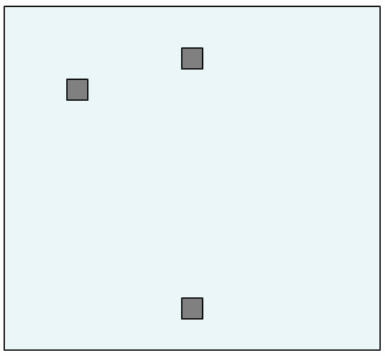
Lithography Level: CONTACT	
	Minimum Feature Size: 3 µm
	Minimum Gap Size: 3 µm
	Material: Aluminum
	Thickness: 5000 Å
	Alignment Tolerance: 10 µm
	GDS Layer Number: 7
	Layer Registration: This layer aligns to the GLASS_RECESS layer. Due to alignment tolerances, the contact pad must be designed at least 5 µm from the edge of a silicon structure.
	Comments: This layer is for creating the ohmic contact to silicon parts for external electrical connections.

Table 2.1.4 - CONTACT Layer

2.2 Detailed Design Rules

2.2.1 GLASS RECESS

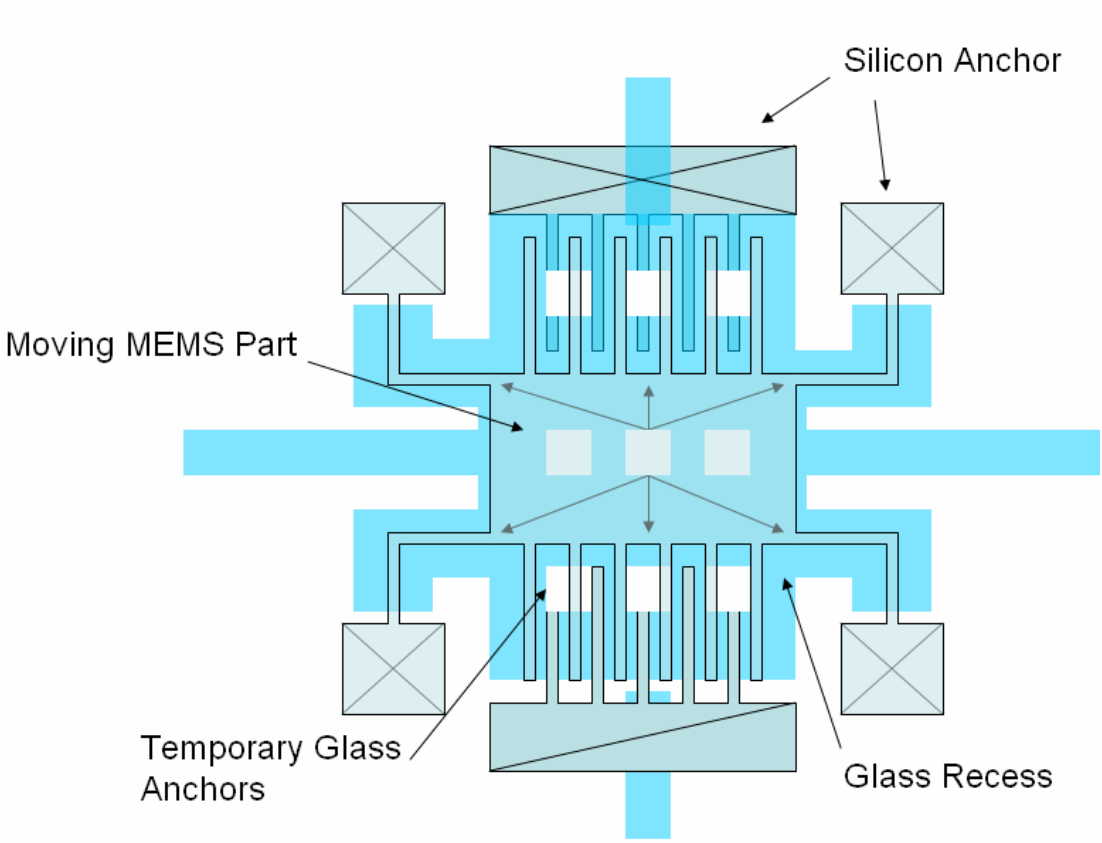


Figure 2.2.1 - Glass recess should be drawn so that it will assure that the moving silicon parts would stay above this glass recess area, taking into account the glass wet etch undercut and backside alignment errors and include the 30um temporary anchors

An example of glass recess underneath moving MEMS parts are shown in Figure 2.2.1. Glass recesses should not be underneath the anchor point taking under consideration glass recess area expansion due to undercut. This defines the minimum gap between the silicon anchor and the edge of the glass recess to be 30 µm. When designing this layer, glass etch undercut must be taken into consideration. For this process, glass undercut is approximately 30 µm.

Note that temporary glass anchors must be present throughout the moving structure. These glass anchors will temporarily secure the moving MEMS part before final release to aid in structural support during dicing as well as heat transfer during DRIE. These glass anchors should be 30 µm squares. During the initial glass etch, the 30 µm squares will etch and be undercut to approximately 10 µm. Then during the final HF release, they will be etched away from the silicon.

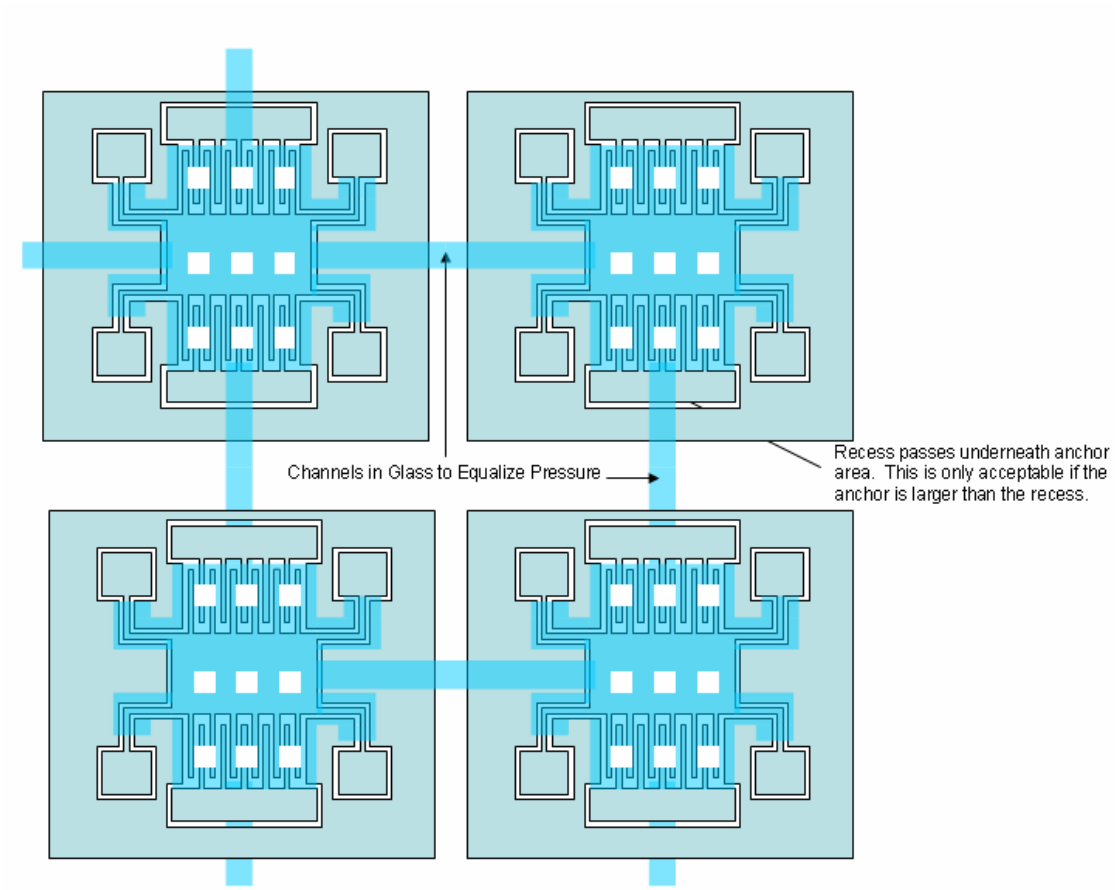


Figure 2.2.2 - Glass recesses within a die must be connected to each other with channels. These channels must also extend at least 200 µm outside of the die.

Glass recesses for moving MEMS structures must have channels that connect them to other recesses within the die which will then run to the dicing lines. This ensures that the pressure inside the glass recesses is equalized with the outside pressure. This is especially important during the release of MEMS devices in the DRIE etch due to the fragility of the released features and possible pressure differentials. Therefore, it is desired that all these recesses for MEMS are connected together with a fluidic channel as shown in Figure 2.2.2. Furthermore, there should be extended fluidic channels at the edges of the die to make fluidic connection to the neighboring dies so that all die are connected with these channels. An extension of 200 µm into the scribe lane is enough for this because by this extension the fluidic channels terminate at the scribe lane on the glass wafer, which cover the entire wafer and connect glass channels of all die with the edges of the wafer. If the channels pass underneath an anchor, the anchor must be defined to be larger than the size of the channel, taking into consideration a 30 µm undercut of the channel width.

2.2.2 SHIELDING METAL ON GLASS

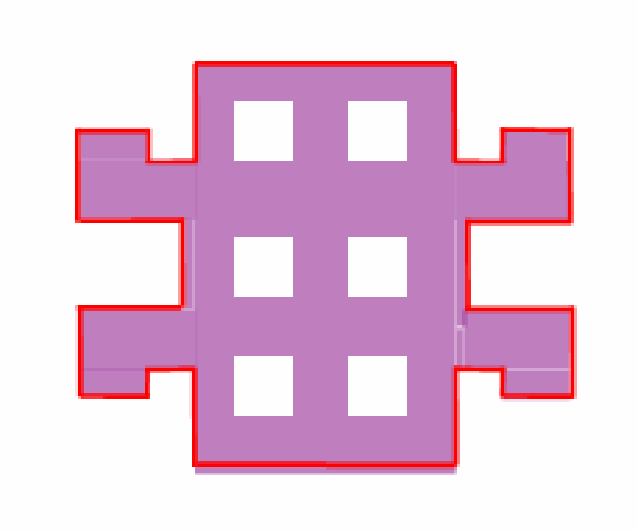


Figure 2.2.3 - Shielding metal on glass will be defined by the GLASS_RECESS mask. Thus, the metal will be precisely inside the glass recess area. This shielding metal will not cause electrical connection of different silicon structures since it will be etched away in the final structure.

The shielding metal layer on glass, as seen in Figure 2.2.3, will be predefined by the GLASS_RECESS masking layer. Thus the metal will be deposited precisely where the glass recess area is. The shielding metal layer will not short different MEMS moving parts that need to be at different potentials because this layer will be eventually removed.

2.2.3 DRIE OF SILICON

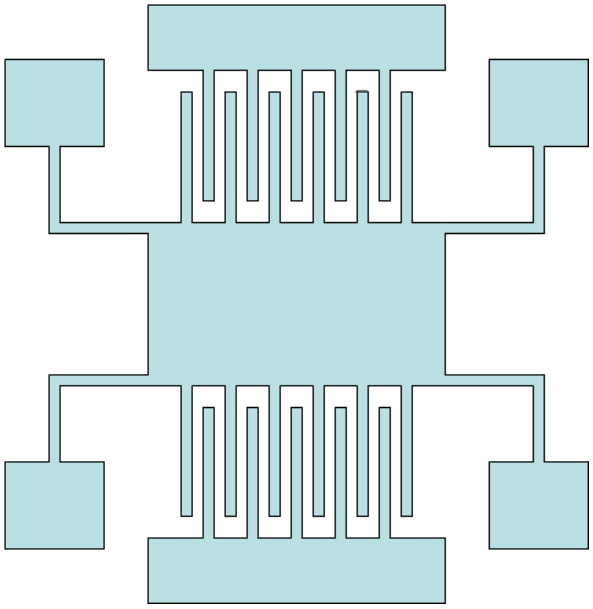


Figure 2.2.4 - A natural instinct is to draw only the MEMS structure. In this example, all of the silicon surrounding it is removed. This structure yields poor uniformity and resolution for the DRIE step

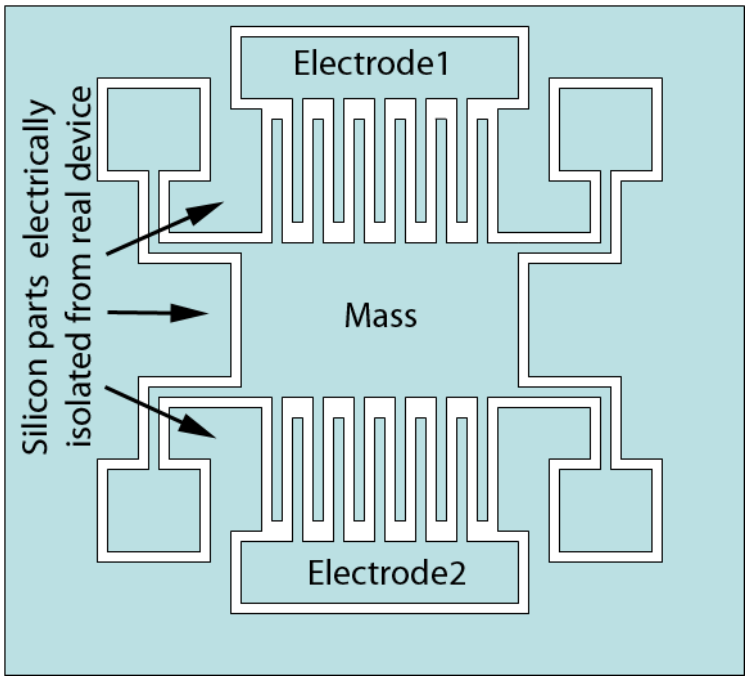
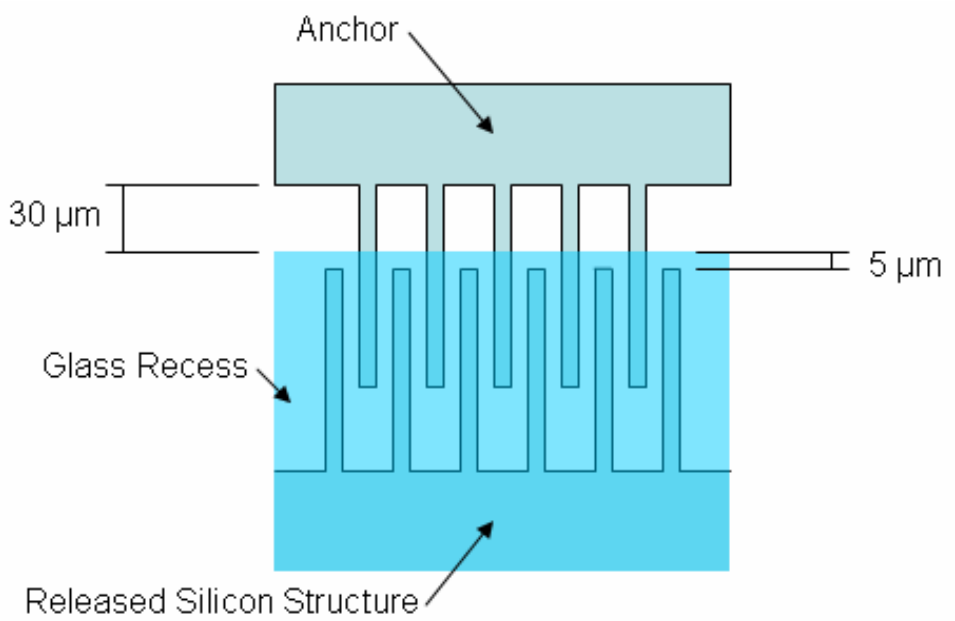


Figure 2.2.5 - The MEMS structure in Figure 2.2.4 should be drawn as seen in this drawing in order to achieve uniform silicon etching and the resolution sought.

In order to have operational MEMS devices and silicon islands, silicon trenches surrounding these structures must be created in the DRIE step. Etching large areas of silicon around these parts will result in non-uniform etching and degrade the profile in the critical small gaps between the silicon parts. In order to insulate the silicon parts, a typical value of 10 µm trenches around the part is enough. The minimum value for this is 5 µm and a maximum value of 10 µm. This design rule is explained for MEMS structures in Table 2.1.1 and Figure 2.2.5.



n

Figure 2.2.6 - The anchor must be 30 µm from the edge of the glass recess and the released silicon structure must be 5 µm from the edge of the recess

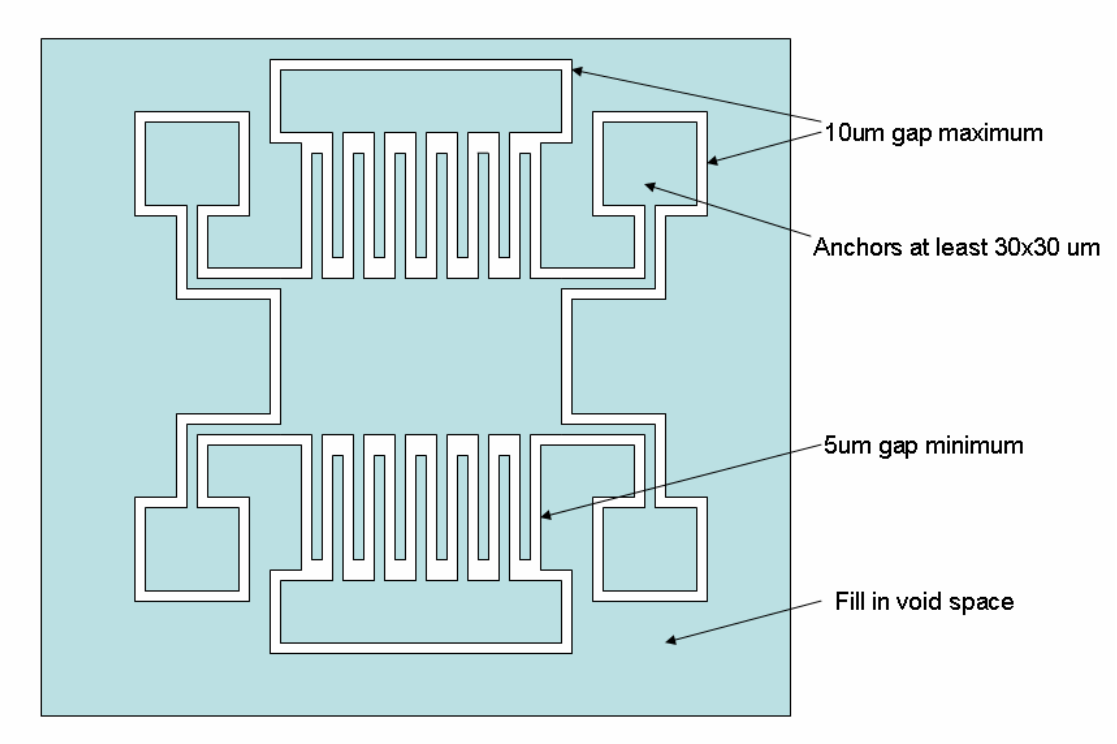
As seen in Figure 2.2.6, the anchor must be at least 30 µm from the edge of the glass recess, due to undercut of the glass and alignment tolerances. Also, the released silicon structure must be at least 5 µm from the edge of the glass recess to ensure that entire structure is over a recessed area.

Note: Long and thin released silicon beams will tend to be deflected out of plane because of some intrinsic stresses in the silicon. Therefore, silicon beams thinner than 6 µm will not survive if they are anchored at one end and they are longer than 100 µm. Beams that are thinner than 6 µm and are anchored at two ends will not survive if they are longer than 500 µm. Beams thicker than 6 µm may survive for very long lengths, as long as 10 mm.

CHAPTER 3

DIAGRAMS

3.1 Detailed Diagrams of layers



3.1.1 - Maximum and minimum allowed features for MEMS device

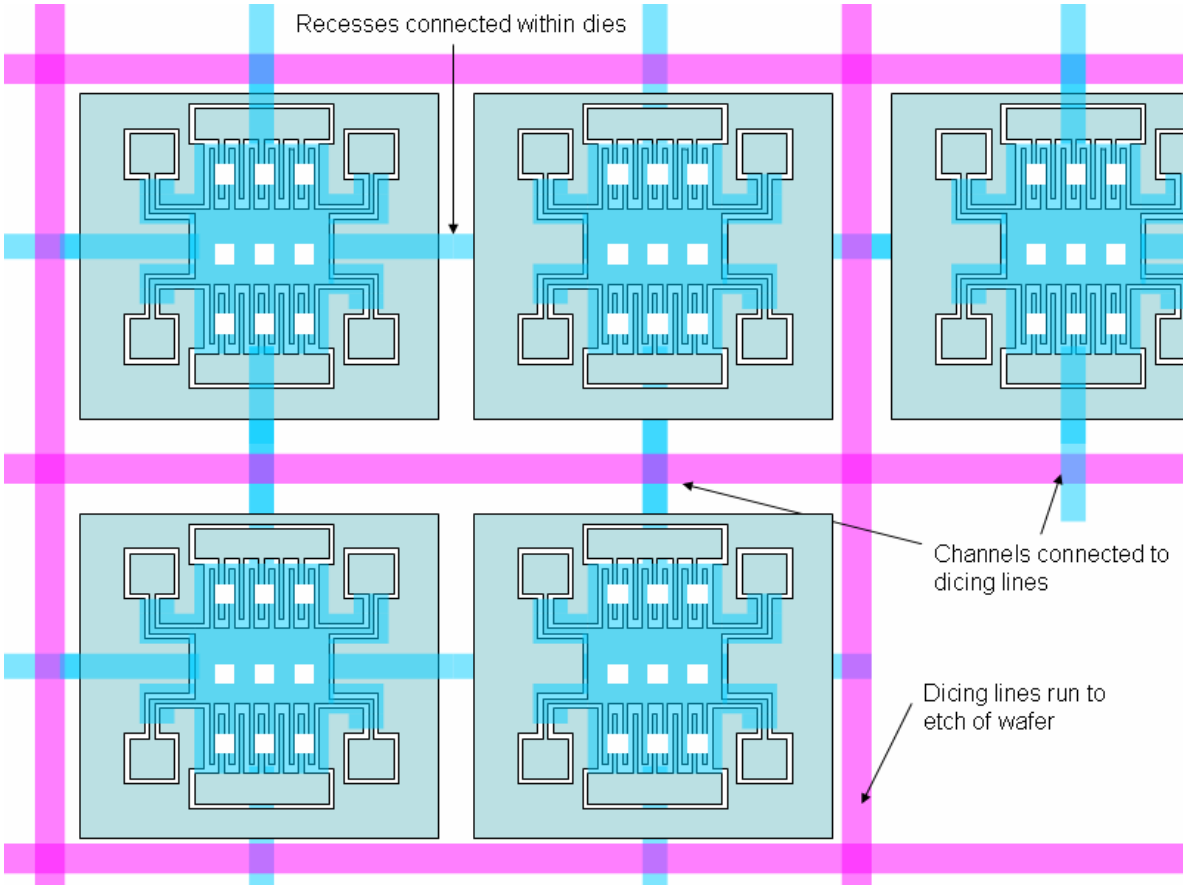


Figure 3.1.2 - Glass recesses should be connected within a die and channels should extend into edge of die and dicing lines

CHAPTER 4

MATERIAL PROPERTIES

4.1 Young's Modulus for Silicon

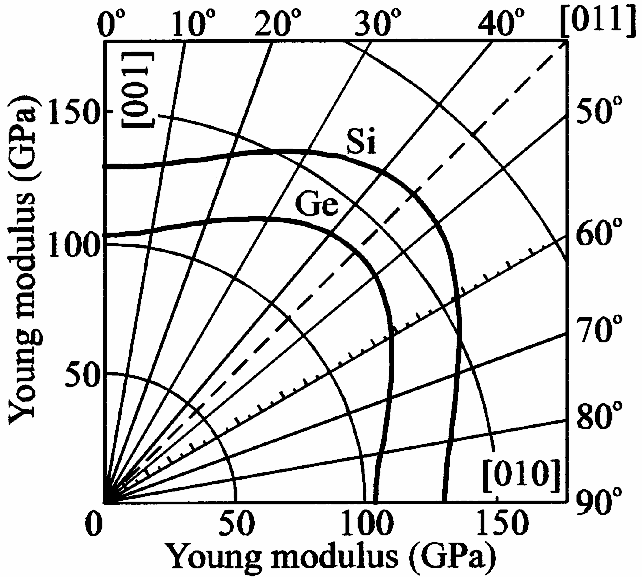


Figure 4.1.1 - Si & Ge Young's Modulus vs. Direction in the <100> plane (Wortman & Evans 1965)

4.2 Capacitance

Capacitance is calculated by the product of permittivity and the surface area divided by the gap between the parallel plates. Refer to Equation 4.2.1.

$$C = \varepsilon_o \frac{A}{d}$$

Equation 4.2.1 - Parallel Plate Capacitance

In this application, the area is calculated by the height multiplied by the length of overlap between the silicon fingers of the mass and anchor. All units are in cm, refer to Equation 4.2.2

$$C = \varepsilon_o \frac{(Height\_of\_silicon\_structure)(Length\_of\_overlap)}{Gap} \text{ x Number of Fingers}$$

Equation 4.2.2 - Parallel Plate Capacitance for MEMS Structure

The permittivity is $\varepsilon_o = 8.854x10^{-12}\,F/cm$ for vacuum and air. The Height_of_silicon_structure is $100x10^{-4}\,cm$, as dictated by the thickness of the silicon wafer. Refer to Figure 4.2.1 for reference to Length_of_overlap.

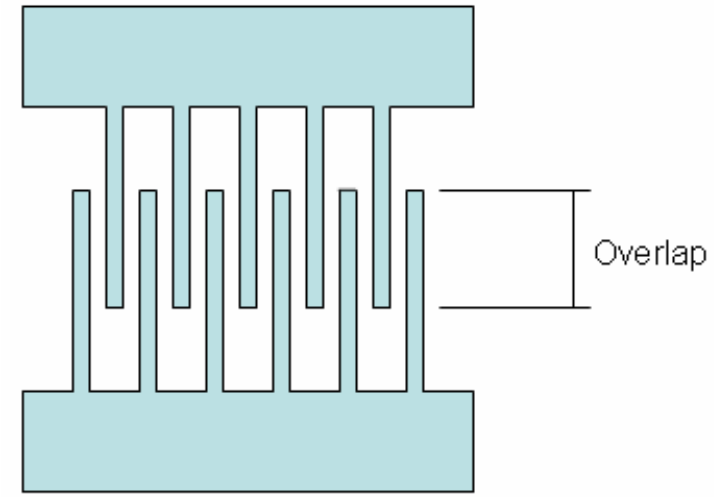


Figure 4.2.1 - This is the section overlap that should be used as the Length_of_overlap